

IN THE CLAIMS

Please cancel claims 2, 5 and 7-10 without prejudice, amend claims 1, 3-4 and 6, and add claims 11-30 as follows:

1 1. (Currently amended) A coding device comprising:
2 a coding circuit configured to generate a coded output from a
3 digital input;
4 an interleaving circuit configured to generate a plurality of
5 interleaved words; and
6 a rate matching circuit for adjusting the number of bits in a
7 data block, the data block comprising a said plurality of
8 interleaved words generated by the action of an interleaving
9 circuit on a coded output generated by the action of a coding
10 circuit on a digital input, the coded output having a greater
11 number of bits than the digital input, the rate matching circuit
12 having means for adjusting the number of bits in the data block
13 using a rate matching pattern to provide data bits for transmission
14 during respective frames of a transmission channel, characterised
15 in that and means are provided for selecting the rate matching
16 pattern depending on the characteristics of the coding circuit and
17 of the interleaving circuit a bit deletion/repetition rate, wherein
18 a bit deletion/repetition pattern is selected to ensure that the

19 deleted or repeated bits are not required to enable all bits from
20 the digital input to be reconstructed.

2. (Canceled)

1 3. (Currently amended) A ~~rate matching circuit~~ coding device
2 as claimed in claim 1 ~~or 2, characterised in that~~, wherein the
3 rate matching pattern for each interleaved word within the data
4 block is offset with respect to the adjacent interleaved word or
5 words within the block.

1 4. (Currently amended) A ~~rate matching circuit~~ coding device
2 as claimed in ~~any one of claims 1 to 3, characterised in that~~,
3 wherein the rate matching pattern is selected as a function of the
4 interleaving depth of the interleaving circuit.

5. (Canceled)

1 6. (Original) A decoding device ~~comprising for decoding a~~
2 signal coded by a coding device ~~as claimed in claim 5~~ having a rate
3 matching circuit for adjusting the number of bits in a data block,
4 the data block comprising a plurality of interleaved words

5 generated by the action of an interleaving circuit on a coded
6 output generated by the action of a coding circuit on a digital
7 input, the coded output having a greater number of bits than the
8 digital input, the rate matching circuit having means for adjusting
9 the number of bits in the data block using a rate matching pattern
10 to provide data bits for transmission during respective frames of a
11 transmission channel, and means for selecting the rate matching
12 pattern depending on a bit deletion/repetition rate, wherein a bit
13 deletion/repetition pattern is selected to ensure that the deleted
14 or repeated bits are not required to enable all bits from the
15 digital input to be reconstructed, and said decoding device
16 comprising a data reconstruction circuit for reconstructing the
17 interleaved words, a de-interleaving circuit and a channel decoder.

Claims 7-10. (Canceled)

1 11.(New) The coding device of claim 1, wherein the rate
2 matching pattern forms a matrix including change bits that indicate
3 change of corresponding bits of said interleaved words within said
4 data block, wherein each row of said matrix includes a maximum of
5 one of said change bits.

1 12.(New) The coding device of claim 1, wherein said coding
2 circuit has one of a fixed code rate and a predetermined number of
3 rates for a variable data source.

1 13.(New) The coding device of claim 1, wherein said
2 interleaving circuit is not adaptive.

1 14.(New) The coding device of claim 1, wherein said
2 interleaving circuit has a constant bit rate.

1 15.(New) The coding device of claim 1, wherein said coding
2 circuit has one of a fixed code rate and a predetermined number of
3 rates for a variable data source, and wherein said interleaving
4 circuit is not adaptive.

1 16.(New) The coding device of claim 1, wherein said rate
2 matching circuit alters a coding rate of said coding circuit.

1 17.(New) A decoding device for decoding a coded digital
2 signal comprising a received data block including interleaved
3 words, said received data block having been processed by a rate
4 matching circuit using a rate matching pattern to adjust a number

5 of bits in said received data block, the decoding device
6 comprising:
7 a data reconstruction circuit having means for adjusting the
8 number of bits in said received data block to reverse action of
9 said rate matching circuit, thereby reconstructing said interleaved
10 words;
11 a de-interleaving circuit having means for generating each of
12 said interleaved words; and
13 a channel decoder which receives said interleaved words
14 provided by said de-interleaving circuit;
15 wherein said rate matching pattern is selected as a function
16 of a bit deletion/repetition rate, a bit deletion/repetition
17 pattern having been selected to ensure that the deleted or repeated
18 bits are not required to enable all bits from the digital input to
19 be reconstructed.

1 18.(New) The decoding device of claim 17, wherein change bits
2 of said rate matching pattern for deleting or repeating bits of
3 said data block are offset with respect to the each other along
4 adjacent rows or columns of a matrix of said rate matching pattern.

1 19.(New) A method of decoding a coded digital signal
2 comprising a received data block including interleaved words, said
3 received data block having been processed by a rate matching
4 circuit using a rate matching pattern to adjust a number of bits in
5 said received data block, the method comprising:
6 adjusting the number of bits in said received data block to
7 reverse action of said rate matching circuit, thereby
8 reconstructing said interleaved words;
9 generating each of said interleaved words; and
10 receiving said interleaved words;
11 wherein said rate matching pattern is selected as a function
12 of a bit deletion/repetition rate, a bit deletion/repetition
13 pattern having been selected to ensure that the deleted or repeated
14 bits are not required to enable all bits from the digital input to
15 be reconstructed.

1 20.(New) The method of claim 19, wherein change bits of said
2 rate matching pattern for deleting or repeating bits of said
3 received data block are offset with respect to the each other.

1 21.(New) The method of claim 19, wherein change bits of said
2 rate matching pattern for deleting or repeating bits of said

3 received data block are offset with respect to the each other along
4 adjacent columns of a matrix of said rate matching pattern.

1 22.(New) The method of claim 19, wherein change bits of said
2 rate matching pattern for deleting or repeating bits of said
3 received data block are offset with respect to the each other along
4 adjacent rows of a matrix of said rate matching pattern.

1 23.(New) The method of claim 19, wherein change bits of said
2 rate matching pattern for deleting or repeating bits of said
3 received data block are offset with respect to the each other along
4 adjacent rows and columns of said rate matching pattern.

1 24.(New) The method of claim 19, wherein said received data
2 block are formed by filling a matrix row by row with row bits of
3 said coded output and outputs column bits of said matrix column by
4 column to form said interleaved words.

1 25.(New) A method of coding a digital signal comprising:
2 generating a coded output from said digital signal;
3 generate a plurality of interleaved words from said coded
4 output; and

5 adjusting the number of bits in a data block comprising said
6 plurality of interleaved words using a rate matching pattern to
7 provide data bits for transmission during respective frames of a
8 transmission channel; and

9 selecting the rate matching pattern depending on a bit
10 deletion/repetition rate, wherein a bit deletion/repetition pattern
11 is selected to ensure that the deleted or repeated bits are not
12 required to enable all bits from the digital input to be
13 reconstructed.

1 26. (New) The method of claim 25, wherein change bits of said
2 rate matching pattern for deleting or repeating bits of said data
3 block are offset with respect to the each other.

1 27. (New) The method of claim 25, wherein change bits of said
2 rate matching pattern for deleting or repeating bits of said data
3 block are offset with respect to the each other along adjacent
4 columns of a matrix of said rate matching pattern.

1 28. (New) The method of claim 25, wherein change bits of said
2 rate matching pattern for deleting or repeating bits of said data

3 block are offset with respect to the each other along adjacent rows
4 of a matrix of said rate matching pattern.

1 29.(New) The method of claim 25, wherein change bits of said
2 rate matching pattern for deleting or repeating bits of said data
3 block are offset with respect to the each other along adjacent rows
4 and columns of said rate matching pattern.

1 30.(New) The method of claim 25, wherein said data block are
2 formed by filling a matrix row by row with row bits of said coded
3 output and outputs column bits of said matrix column by column to
4 form said interleaved words.